MCF52110 Chip Errata

Silicon Revision: All

This document identifies implementation differences between the MCF5211*x* processors and the description contained in the *MCF52110 ColdFire® Reference Manual*. Refer to http://www.freescale.com/coldfire for the latest updates.

Table 1. Summary of MCF5211x Errata

Errata	Module Affected	Date Errata Added	Revision Affected?
			MCF5211x
SECF015	Flash	11/17/06	Yes
SECF018	ADC	2/5/08	Yes
SECF019	ADC	2/5/08	Yes
SECF014	BDM	3/20/08	Yes
SECF194	OSC	4/05/11	Yes
SECF195	OSC	4/05/11	Yes

The table below provides a revision history for this document.

Table 2. Document Revision History

Rev. No.	Date	Substantive Changes
0	3/2008	Initial release
1	3/2008	Added SECF014

Table continues on the next page...

Table 2. Document Revision History (continued)

Rev. No.	Date	Substantive Changes
2	3/2009	Added SECF015
3	5/2009	Removed previously added SECF134, as this device does not contain a USB module.
4	4/2011	Added SECF194
4	4/2011	Added SECF195
5	02/2015	Updated SECF015
6	07/2015	Removed fix plan information from the fix plan section of SECF015. There are no plans to fix SECF015 on this device.

SECF018: ADC Might Give Erroneous Results if V_{REFH} and V_{REFL} are Not at the Same Potential as V_{DDA} and V_{SSA} Respectively

Errata type: Silicon
Affects: ADC
Description: The ADC could produce an error if the ADC reference voltage VREFH is below the analog supply voltage VDDA, or if the ADC reference voltage VREFL is above analog ground VSSA by more than 50 mV. The error is that the ADC digital result might jump randomly to an invalid value before returning to a correct value on the next result. The invalid value could be full scale (for example, 0 or 4095) or mid range.

Workaround: Connect V_{REFH} directly to V_{DDA}. Similarly, connect V_{REFL} to V_{SSA}.

Fix plan: Currenty, there are no plans to fix this.

SECF019: ADC Might Give Erroneous Results if the ADC Reference Voltage (V_{REFH}) is Below 3.1 V

Errata type: Silicon
Affects: ADC
Description: If the ADC reference voltage V_{REFH} is less than 3.1 V, either of the following error conditions could result:

- Low analog input voltages to the ADC might not be measured properly. (for example, input voltages less than 100 mV might yield measurements equal to 0)
- The ADC digital result might jump randomly to an invalid value before returning to a correct value on the next result. The invalid value could be full scale (for example, 0 or 4095) or mid range.

Workaround: Ensure that V_{REFH} is at or above 3.1 V.

Fix plan: Currenty, there are no plans to fix this.

SECF014: Level 2 Trigger Operation Controlled by TDR[31]

Errata type: Silicon
Affects: BDM
Description: The TDR[L2T] bit (TDR bit 15) has no effect on the level 2 trigger. Bit 31 of the TDR register provides both trigger response control and logical operation of the level 2 trigger.

Workaround: Use the TDR[31] bit to control the logical operation for the level 2 trigger as follows:

- 0 -- Level 2 trigger = PC_condition & Address_range & Data_condition
- 1 -- Level 2 trigger = PC_condition | (Address_range & Data_condition)

Since TDR[31] is also part of the trigger response control, only certain combinations of trigger responses and logical operations are available as shown below:

Table 3. TDR[31:30] Definitions

TDR[31:30]	Level 2 Trigger	Trigger Response
00	PC_cond & (Add_range & Data_cond)	Display on DDATA
01		Processor halt
10	PC_cond | (Add_range & Data_cond)	Debug interrupt
11		Reserved

Fix plan: Currently, there are no plans to fix this.

SECF015: Internal Flash Speculation Address Qualification Incomplete

Errata type: Silicon
Affects: Flash controller
Description: The flash controller uses a variety of advanced techniques, including two-way 32-bit bank interleaving, address speculation, and pipelining to improve performance. An issue involving a complex series of interactions between the local flash controller and other memory accesses (internal SRAM, EIM, or SDRAM) has been uncovered. In rare instances, the interaction between a non-flash memory access and a flash access can result in incorrect data usage for a read operation. This may produce unexpected exceptions, incorrect execution, or silent data corruption.

The problem requires two accesses where the modulo (flash size) address and address mask configuration are the same for both a flash access and a non-flash access that occur close in time.

Workaround: **Workaround Step 1 (Always do this)**: Use FLASHBAR[6] to disable the address speculation mechanisms of the flash controller. The default configuration (FLASHBAR[6] = 0) enables the address speculation. If FLASHBAR[6] equals 1, address speculation is disabled. Core performance may be degraded from 4% – 9%, depending heavily on application code.

NOTE

FLASHBAR[6] is user accessible via the movec instruction.
FLASHBAR[6] always reads back as 0.

NOTE

On MCF528x and MCF521x devices FLASHBAR[6] is already set to 1 for datecodes XXX0327 and later. The bit still reads back as 0.

Workaround Step 2a (Select one of the step 2 options to use): Construct the device memory map so the flash and SRAM spaces are disjoint within the modulo-(flash_size) addresses. In some cases if this approach is selected, the upper portion of the flash memory might be unused and the SRAM be mapped to this unused flash space.

Consider an example where the flash memory size is 256 Kbytes and the on-chip SRAM size is 32 Kbytes. If 224 Kbytes or less of flash are used, the SRAM can be based at the upper 32 Kbytes (within the modulo-256 Kbyte address) of the flash address space:

```
Flash: size = 0x40000, base = 0x0000_0000
RAM: size = 0x08000, base = 0x8003_8000 = RAM_BASE+(256-32) Kbytes
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where the flash and SRAM base addresses are unique BA[31:16].

In summary, this approach can be applied if the combined size of the used flash and used SRAM is less than the total flash size, with the flash contents justified to the lower address range and the SRAM contents justified to the upper address range.

Workaround Step 2b (Select one of the step 2 options to use): Separate the contents of the SRAM and the flash memory into exclusive categories and use the address space mask bits in FLASHBAR and RAMBAR to restrict accesses. For example, if the flash contains only instructions and the SRAM contains only operands (all data), the appropriate address space mask fields are specified to prevent flash and SRAM accesses from overlapping.

Workaround Step 3a (Select one of the step 3 options to use if external parallel memory is used in the system): Do not enable caching of external memories. With caching disabled the timing requirements for an issue to occur will not be met, so this will prevent conflicts between flash and external parallel memory accesses through the EIM or SDRAMC.

Workaround Step 3b (Select one of the step 3 options to use if external parallel memory is used in the system): Separate the contents of the EIM and/or SDRAM and the flash memory into exclusive categories and use the address space mask bits in FLASHBAR, CSMRn, and DMRn to restrict accesses. For example, if the flash contains only instructions and the SDRAM contains only operands (all data), the appropriate address space mask fields are specified to prevent flash and SRAM accesses from overlapping.

Fix plan: Currently, there are no plans to fix this.

SECF194: OSC: Intermittent operation of crystal oscillator over full temperature range with greater than 25 MHz crystal.

Errata type: Silicon
Affects: Oscillator
Description: If a crystal frequency greater than 25 MHz is used, the crystal oscillator voltage may decay to a very low amplitude over a narrow temperature range. The exact temperature range is implementation specific and is dependent upon the crystal, the crystal load capacitors, and the board layout. In some cases the very low oscillator voltage amplitude may cause the device to reset.

Workaround: It is recommended that the following action be taken to avoid problems:

Perform negative resistance test on the crystal oscillator circuit to determine level of margin. Margin level is measured resistance at room temperature divided by the series resistance of the crystal. If margin is below 2 make circuit changes as detailed here.

If the margin is below 2, perform one of the following actions:

1. Change the clock source to an external clock and make appropriate mode select changes, or
2. Use a crystal of 25 MHz or less.

Fix plan: No plans to fix.

SECF195: OSC: Limited input voltage range on EXTAL pin.

Errata type: Silicon
Affects: Oscillator
Description: The input circuit of the EXTAL pin should be limited to 3.0 V. Failure to keep the voltage below 3.0V may lead to a decrease in lifespan of the device.

Workaround: It is recommended that the following action be taken to avoid problems:

- Ensure that the maximum voltage on EXTAL is below 3.0V. Use a resistor divider or other method to keep input voltage on EXTAL pin below 3.0V.

Fix plan: No plans to fix.

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